Title of the Invention

Ins A1 Semiconductor Integrated Circuit

Background of the Invention

The present invention relates to a voltage converter which lowers an external supply voltage within a semiconductor integrated circuit chip. Ins B1

Reduction in the B1 geometries of devices such as bipolar or MOS transistors has been accompanied by a ~~attended with~~ lowering in the breakdown voltages of the devices, which has made it necessary ~~inevitable~~ to lower the operating voltage of small geometry devices with an integrated circuit ~~correspondingly~~. From the viewpoint of users, however, a single voltage source of, for example, 5 V, which is easy to ~~of~~ use is desirable. As an expedient for meeting such different requests of IC manufacturers and the users, it is considered to be neccessary to lower the external supply voltage V_{CC} within a chip and to operate the small geometry devices with the lowered voltage V_L.

Figure 1 shows an example of such an ~~the~~ expedient, in which the circuit A' of the whole chip 10 including, e. g., an input/output interface circuit is operated with the internal supply voltage V_L lowered by a voltage converter 13.

Figure 2 shows an integrated circuit disclosed in B2 ~~Japanese Patent Application No. 56-57143 (Japanese Laid-open Patent Application No. 57-172761)~~. The small Ins B2

geometry devices are employed for a circuit A determining the substantial density of integration of the chip 10, and are operated with the voltage V_L obtained by lowering the external supply voltage V_{CC} by means of a voltage converter 13. On the other hand, devices of comparatively large geometries are employed for a driver circuit B including, e. g., an input/output interface which does not greatly contribute to the density of integration~~.~~ which ~~and they~~ are operated by applying V_{CC} thereto. Thus, a large-scale integrated circuit (hereinbelow, termed "LSI") which operates with V_{CC} when viewed from outside the chip becomes possible.

However, when such an integrated circuit is furnished with the voltage converter, an inconvenience is involved in an aging test which is performed after the final fabrication step of the integrated circuit.

The terminology "aging test" ~~is such that,~~ after the final fabrication step of the integrated circuit~~,~~ during which voltages higher than in an ordinary operation are intentionally applied to the respective transistors in the circuit~~.~~ ~~thereby~~ to test the integrated circuit ~~which is liable~~ for ~~to~~ break down due to an inferior gate oxide film.

The aforementioned voltage converter in Japanese Patent Application No. 56-57143 functions to feed the predetermined voltage. Therefore, the circuit fed with

the supply voltage by the voltage converter cannot be subjected to the aging test.

b In order to solve this problem, an invention disclosed in U.S. Patent 4,482,985 ~~Japanese Patent Application No. 56-168698~~ has previously been made, but it has had difficulty in the performance for actual integrated circuits. As illustrated in Figures 2 b to 6 in the patent ~~application~~, according to that ~~the~~ cited invention, an internal voltage increases up to an aging point rectilinearly or with one step of change as an external supply voltage increases. Accordingly, the internal voltage changes greatly with the change of the external supply voltage. This has led to the disadvantage that the breakdown voltage margins of small geometry devices in an ordinary operation become small.

Summary of the Invention

b An object of the present invention is to further advance the invention disclosed in U.S. Patent 4,482,985 ~~Japanese Patent Application~~ b ~~No. 56-168698~~ referred to above, and to provide a voltage Ins C1 converter ~~which~~ can widen the margins of the breakdown voltages of small geometry devices in an ordinary operation and which affords sufficient voltages in an aging test.

c The present invention consists in that the output voltage of the ~~a~~ voltage converter is set at a voltage suitable for the operations of small geometry devices against the change of an external supply voltage when a semiconductor

integrated circuit is in its ordinary operation region, and at an aging voltage when the ordinary operation region is exceeded.

To this end, according to the voltage converter of the present invention, when the external supply voltage has been changed from the lower limit value of the ordinary operation range thereof to the aging operation point thereof, the output voltage of the voltage converter changes up to the aging voltage without exhibiting a constant changing rate versus the change of the external supply voltage.

Brief Description of the Drawings

Figures 1 and 2 show semiconductor integrated circuits each having a voltage converter.

Figures 3 and 5 show basic circuits each of which constitutes a device embodying the present invention.

Figures 4 and 6 show the characteristics of the circuits in Figures 3 and 5, respectively.

Figures 7, 9 and 11 show devices embodying the present invention.

Figures 8, 10 and 12 show the characteristics of the circuits in Figures 7, 9 and 11, respectively.

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Figures ~~13~~ 13 (A) to (C), and ~~14~~ 14 (A) to (C) show B4 the formation of the circuit of Figure 3 in practicable forms. B5

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Figure 15 shows the characteristic in Figure 4

more specifically.

Figure 16 shows another practicable example of the circuit in Figure 3.

Figure 17 shows the characteristic in Figure 8 concretely.

Figure 18 shows a circuit for producing the characteristic in Figure 17.

Figure 19 shows the characteristic in Figure 8 concretely.

Figure 20 shows a circuit for producing the characteristic in Figure 19.

Figure 21 shows the characteristic in Figure 10 concretely.

Figure 22 shows a circuit for producing the characteristic in Figure 21.

Figure 23 shows a characteristic in another embodiment of the present invention.

Figure 24 shows a circuit for producing the characteristic in Figure 23.

Figure 25 shows the characteristic in Figure 12 concretely.

Figure 26 shows a circuit for producing the characteristic in Figure 25.

Figure 27 shows a practicable example of the circuit in Figure 26.

Figure 28 shows the actual characteristics of the circuit in Figure 27.

Figure 29(A) shows a gate signal generator for use in an embodiment of the present invention.

Figure 29(B) shows a time chart of the circuit in Figure 29(A).

Figure 30 shows a protection circuit which connects the circuit of Figure 29(A) with the circuit of Figure 16, 18, 20, 22, 24 or 26.

Figure 31 shows a practicable circuit of an inverter for use in the circuit of Figure 29(A).

Figure 32 shows a practicable circuit of an oscillator for use in the circuit of Figure 29(A).

Figure 33 shows an example of a buffer circuit for the output of the circuit shown in Figure 16, 18, 20, 22, 24 or 26.

Figure 34 shows the characteristics of the circuit in Figure 33.

Figures 35, 36 and 37 show other examples of buffer circuits, respectively.

Figure 38 shows a time chart of the circuit in Figure 37.

Figure 39 shows a practicable example of the circuit in Figure 3.

Figure 40 shows an example of a buffer circuit.

Figure 41 shows the characteristics of the circuit in Figure 40.

Description of the Preferred Embodiments

Voltage converter circuit forms for affording various output characteristics versus an external supply voltage V_{CC}, as well as practicable examples thereof, will be first described, followed by practicable embodiments on a method of feeding power to the voltage converter and on a buffer circuit for the voltage converter well suited to drive a high load. C2

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Figures 3 and 5 show basic circuits each of which constitutes the voltage converter of the present invention.

In the circuit of Figure 3, a resistance R_3 in Figure 13 ~~14~~ of U.S. Patent 4,482,985 ~~Japanese Patent Application No. 56-168698~~ already filed is made variable, and a transistor Q is employed in order to enhance a current driving ability for a load to which an output voltage V_L is applied. Here, the control terminal voltage V_G of the transistor Q has a characteristic which changes versus the change of an external supply voltage V_{CC} and which is the output voltage of a reference voltage generator REF. More specifically, as illustrated in Figure 4, in a case where the external supply voltage V_{CC} is gradually increased from 0 (zero) V, the voltage V_G rises abruptly when a certain voltage V_P has been reached, so that the transistor Q

b

turns "on". For V_{CC} not smaller than V_P, Q continues to turn "on". Therefore, the effective impedance of the whole basic circuit BL decreases ~~lowers~~, and the ratio thereof with the effective impedance R changes, so that the voltage V_L becomes a straight line of different slope for V_{CC} not smaller than V_P as shown in Figure 4. Here in Figure 4, the example is illustrated in which V_G rises abruptly from 0 V to a certain voltage for V_{CC} not smaller than V_P. However, it is also allowed to adopt a characteristic in which, in case of changing V_{CC} from 0 V, V_G rises gradually from 0 V and becomes, at the point V_P, a voltage level to turn "on" the transistor Q. Regarding the example in which V_G rises abruptly at and above the certain voltage V_{CC}, the reference voltage generator can be realized by the cascade connection of devices having rectification characteristics as taught in U.S. Patent 4,482,985 ~~Japanese Patent Application No. 56-168698~~. Regarding the example in which V_G rises gradually, the reference voltage generator can be realized by a simple resistance divider circuit. In Figure 4, the coefficient of V_L relative to V_{CC} can be changed at will by the designs of the resistance and the transistor Q.

Figure 5 shows another example which employs the same basic circuit BL as in Figure 3. Whereas the example of Figure 3 derives V_L from the V_{CC} side, this example

derives V_L from the ground side. When the characteristic of the output voltage V_G from the reference voltage generator is set in advance so that the transistor Q may turn "on" at V_{CC} not smaller than V_P, V_L is determined by the effective impedance of the whole basic circuit BL and the effective impedance R, and hence, V_L becomes as shown in Figure 6.

While Figures 3 and 5 have exemplified the transistors as being ~~the~~ MOS transistors, bipolar transistors may ~~well~~ be used if desired. Particularly in a case where ~~the~~ whole chips are constructed of MOS transistors in the examples of Figures 1 and 2, it is usually easier to design them when the circuits of Figures 3 and 5 are constructed of MOS transistors. In a case where the whole chips are of bipolar transistors, it is more favorable to use bipolar transistors. It is sometimes the case, however, that the chip includes both MOS transistors and bipolar transistors. It is to be understood that, in this case, the MOS transistor or/and the bipolar transistor can be used for the circuit of Figure 3 or Figure 5 in accordance with an intended application. In addition, although the examples of Figures 4 and 6 have been mentioned as the characteristics of the circuit REF, these examples are not especially restrictive, but the characteristic of the circuit REF may be set according to the purpose

of the design of V_L.

Now, the voltage converter based on the circuit of Figure 3 will be described. Figures 7 and 8 illustrate an example in which the basic circuits BL numbering k are connected in parallel with the effective impedance R of the circuit of Figure 3. The circuits REF in the respective basic circuits BL are set so that BL_0 may first turn "on" at V_{P0}, BL_1 may subsequently turn "on" at V_{P1}, and BL_k may lastly turn "on" at V_{Pk}. The transistors in the respective circuits BL are designed so that the coefficients of the changes of the respective voltages V_L versus the voltage V_{CC} may be varied. As V_{CC} increases more, impedances are successively added in parallel with the impedance R, so that the entire characteristic of V_L becomes concave for V_{CC} not smaller than V_{P0}.

The coefficients of the changes are varied for the following reason. For example, in a case where the aging operation points are V_{P2}, V_{P3}, ... and V_{Pk} and where the aging voltages of circuits to be fed with the supply voltages by the voltage converter are V_{L2}, V_{L3}, ... and V_{Lk}, the transition is smoothed when the first aging operation point shifts to the next one.

The present circuit is a circuit which is practical in points of the operating stability of the ordinary operation and an effective aging for the system of Figure 2.

By way of example, the V_{CC} operation point in the ordinary operation is set at a point at which V_L changes versus V_{CC} as slightly as possible, that is, the coefficient of change is the smallest, in order to achieve a stable operation, whereas the V_{CC} operation point in the aging test is set at a point at which the coefficient of change is great, in order to approximately equalize the stress voltage conditions of a transistor of large geometry and a transistor of small geometry as described in Japanese Patent Application No. 56-168698. More concretely, in case of using only BL_0 and BL_1 in the circuit of Figure 7, the coefficient of change in Figure 8 may be made small between the lower limit voltage V_{P0} (e. g., 2 - 3 V) and the upper limit voltage V_{P1} (e. g., 6 V), to set the ordinary operation point (e. g., 5 V) concerning V_{CC} for the ordinary operation range in this section, while the coefficient of change may be made great between
18 V_{P1} and V_{P2} (e. g., 7 - 9 V), to set the aging operation point (e. g., V_{CC} = 8 V) in this section. The ordinary operation range is solely determined by ratings, and it is usually set at 5 ± 0.5 V. It is to be understood that, for some purposes of designs, the operation voltage points and the aging voltage points can be set at any desired V_{CC} points by employing the basic circuits BL_2, BL_3 ··· more. When the more circuits BL are used, the

V_L characteristic can also be made smoother versus V_{CC}, so that the operation of the internal circuit can be stabilized more. Further, since the V_{CC} voltage is high in the aging test, it is effective to construct the voltage converter itself by the use of high breakdown voltage transistors. To this end, the voltage converter may be constructed of transistors of large geometry in the system of Figure 2 by way of example.

Figures 9 and 10 show an example in which the basic circuits BL are connected in parallel on the ground side. As stated before, when the respective circuits BL are properly designed, the characteristic of the whole V_L can be made convex relative to V_{CC}. This characteristic is effective for protecting the circuit A' from any overvoltage V_L in the system of Figure 1 by way of example. This achieves the advantage that, in case of measuring the V_{CC} voltage margin of the whole chip, a sufficiently high voltage V_{CC} can be applied without destroying small geometry devices.

In some uses, it is also possible that the circuits of Figures 7 and 9 coexist. By way of example, the ordinary operation point is set at a point at which the coefficient of change is small, and the aging operation point is set at a point at which the coefficient of change is great. These are realized by BL_0 and BL_1 in

the circuit of Figure 7. Further, in order to make the coefficient of change small again at and above the V_{CC} point of the aging condition to the end of preventing the permanent breakdown of devices, the basic circuits BL other than BL_O are connected so as to operate in parallel with the latter as in the circuit form of Figure 9. This makes it possible to design a circuit in which the devices are difficult to break down at and above the V_{CC} point of the aging condition.

Thus, even when the supply voltage has been made abnormally high erroneously by way of example, the breakdown of the devices can be prevented.

Figures 11 and 12 show an example in which a basic circuit BL' is connected in parallel with the circuit of Figure 3, whereby the changing rate of V_L is made negative at and above V_P' which is a certain value of V_{CC}. More specifically, when V_{CC} is increased, the transistor Q first turns "on" while the output voltage V_G of the reference voltage generator 1 in the basic circuit BL is not lower than V_P, so that the gradient of V_L versus V_{CC} decreases. A reference voltage generator 2 is designed so that a transistor Q' in the basic circuit BL' may subsequently turn "on" at the certain V_{CC} value, namely, V_P'. In addition, the conductance of Q' is designed to be sufficiently higher than that of Q. Then,

the V_L characteristic after the conduction of the transistor Q' is governed by the characteristic of BL', so that V_L comes to have the negative gradient as shown in Figure 12.

The merit of the present circuit is that, when the aforementioned point at which V_L lowers is set at or below the breakdown voltages of small geometry devices, these small geometry devices are perfectly protected from breakdown even when the voltage V_{CC} has been sufficiently raised. For example, a measure in which the output voltage V_L lowers when a voltage higher than the external supply voltage V_{CC} at the aging point has been applied is especially effective because any voltage exceeding the aging point is not applied to the devices.

It is to be understood that an external instantaneous voltage fluctuation can also be coped with.

Obviously, the circuit of Figure 5 can afford any desired V_L characteristic by connecting the basic circuit BL' in parallel as in the example of Figure 3.

While, in the above, the conceptual examples of the voltage converters have been described, practicable circuit examples based on these concepts will be stated below.

Figure 13 shows a practicable example of the circuit of Figure 3 which employs a bipolar transistor. A voltage regulator circuit CVR is, for example, a cascade

connection of Zener diodes or ordinary diodes the terminal voltage of which becomes substantially constant. (A) indicates a well-known voltage regulator. This is described in detail in "Denpa-Kagaku (Science of Electric Wave)", February 1982, p. 111 or "Transistor Circuit Analysis", by Joyce and Clarke, Addison-Wesley Publishing Company, Inc., p. 207. Since, however, V_L is a fixed voltage in this condition, a resistance r is connected in series with CVR as shown in (B). Thus, V_L comes to have a slope relative to V_{CC} as shown in (C).

Figure 14 shows another embodiment. (A) indicates a well-known voltage regulator which employs an emitter follower. Since V_L is also a fixed voltage, a resistance r is used in (B) as a measure of solution. Thus, a characteristic as shown in (C) is afforded.

These examples of Figures 13 and 14 are especially suited to the system as shown in Figure 1. In Figure 1, usually a great current flows through the circuit associated with the input/output interface. Therefore, a high current driving ability is required of the voltage converter correspondingly. Obviously, the voltage converter constructed of the bipolar transistor is suited to this end.

Next, there will be explained practicable examples in which voltage converters are constructed of MOS transistors on the basis of the circuits of Figures 3, 7, 9 and 11.

Figure 15 shows a concrete example of the characteristic of Figure 4 in which V_L is endowed with a slope $\underline{m}$ for V_{CC} of and above a certain specified voltage V_O. Since the change of V_L decreases for the voltage not smaller than V_O, the breakdown of small geometry devices becomes difficult to occur to that extent.

$V_L = V_{CC}$ is held for V_{CC} smaller than V_O, for the following reason. In general, MOSTs have the operating speeds degraded by lowering in the threshold voltages thereof as the operating voltages lower. To the end of preventing this drawback, it is desirable to set the highest possible voltage on a lower voltage side such as V_{CC} smaller than V_O. That is, V_L should desirably be equal to V_{CC}.

Figure 16 shows an embodiment of a practicable circuit DCV therefor, which corresponds to a practicable example of the circuit of Figure 3.

The features of the present circuit are that the output voltage V_L is determined by the ratio of the conductances of MOS transistors Q_O and Q_ℓ, and that the conductance of the MOS transistor Q_ℓ is controlled by the output voltage V_L.

With the present circuit, letting the gate voltage V_G of Q_O be $V_{CC} + V_{th(O)}$ (where $V_{th(O)}$ denotes the threshold voltage of the MOST Q_O), the control starting voltage V_O

and the slope m are expressed as follows:

$$V_O = \sum_{i=1}^{n} V_{th(i)} + V_{th(\ell)}$$

$$m = \left\{1 + \sqrt{\beta(\ell)/\beta(0)}\right\}^{-1}$$

Here, $\beta(0)$ and $\beta(\ell)$ denote the channel conductances of Q_0 and Q_ℓ, $V_{th(i)}$ ($i = 1 - n$) and $V_{th(\ell)}$ denote the threshold voltages of the MOS transistors Q_i ($i = 1 - n$) and Q_ℓ, and n denotes the number of stages of Q_i.

Accordingly, V_O and m can be varied at will by n, $V_{th(i)}$, $V_{th(\ell)}$ and $\beta(\ell)/\beta(0)$. It has been stated before that $V_L = V_{CC}$ is desirable for V_{CC} smaller than V_O. In this regard, for V_{CC} smaller than V_O, V_L is determined by V_O because Q_ℓ is "off". Therefore, the voltage V_G of Q_0 must be a high voltage of at least $V_{CC} + V_{th(0)}$.

In order to simplify the computation and to facilitate the description, the circuit of Figure 16 is somewhat varied from an actual circuit. As a practical circuit, as shown in Figure 27 to be referred to later, a transistor of similar connection ($Q_{S(1.6)}$ in Figure 27) needs to be further connected between the n-th one of the transistors connected in cascade and the ground. That is, a kind of diode connection is made toward the ground. With this measure, when V_{CC} has been varied from the high

voltage side to the low voltage side, the nodes of the transistors connected in cascade are prevented from floating states to leave charges behind. For the sake of the convenience of the description, the transistor of this measure shall be omitted in the ensuing embodiments.

Figure 17 shows a characteristic in which, when the external supply voltage V_{CC} changes between the lower limit value V_O and upper limit value V_O' of the ordinary operation range, the slope m of the output voltage V_L is small, and a slope m' which corresponds to the external supply voltage greater than V_O' is made steeper than m.

Figure 18 shows an example of a circuit for producing the characteristic of Figure 17.

These correspond to a practicable form of the example of Figures 7 and 8.

The feature of the present circuit is that, between the terminals 1 and 2 of the circuit DCV shown in Figure 16, a circuit DCV2 similar to DCV1 is added, whereby the conductance of a load for DCV1 is increased at and above V_O' so as to increase the slope of V_L.

With the present circuit, the second control starting voltage V_O' is expressed by:

$$V_O' = V_O + \left\{\sum_{i=1}^{n} V_{th(i)} + V'_{th(\ell)}\right\}/(1 - m)$$

In addition, the slope m' is determined by the ratio between the sum of the conductances of the MOS transistors Q_O and Q'_ℓ and the conductance of the MOS transistor Q_ℓ. Here, $V'_{th(i)}$ (i = 1 - n') and $V'_{th(\ell)}$ denote the threshold voltages of the MOS transistors Q'_i (i = 1 - n') and Q'_ℓ, respectively.

Accordingly, V'_O and m' can be varied at will by n, n', $\beta(\ell)$, $\beta'(\ell)$, $V_{th(i)}$, $V_{th(\ell)}$, $V'_{th(i)}$ and $V'_{th(\ell)}$. Here, $\beta'(\ell)$ denotes the channel conductance of the MOS transistor Q'_ℓ.

This circuit has the ordinary operation range between the lower limit value V_O and the upper limit value V_O', and is effective when the aging point has a value larger than V_O'. That is, since the slope m is small in the ordinary operation region, margins for the breakdown voltages of small geometry devices are wide, and power consumption does not increase. Here, the slope m' for the external supply voltage higher than the ordinary operation region is set for establishing a characteristic which passes an aging voltage (set value).

In an example illustrated in Figure 19, a characteristic in which the slope of V_L becomes m" greater than m' when the external supply voltage V_{CC} has reached V_O'' is further added to the characteristic shown in Figure 17.

Figure 20 shows an example of a practicable circuit

therefor. These correspond to a concrete form of the example of Figures 7 and 8. The feature of the present circuit is that circuits DCV2 and DCV3 similar to the circuit DCV1 are added between the terminals 1 and 2 of the circuit shown in Figure 16, whereby the conductance of the load for DCV1 is successively increased so as to increase the slope of V_L in two stages at the two points V_O' and V_O''.

With the present circuit, the second and third control starting voltages V_O' and V_O'' are respectively expressed by:

$$V_O' = V_O + \{\sum_{i=1}^{n'} V'_{th(i)} + V'_{th(\ell)}\}/(1 - m)$$

$$V_O'' = V_O' + \{\sum_{i=1}^{n''} V''_{th(i)} + V''_{th(\ell)} - \sum_{i=1}^{n'} V'_{th(i)} - V'_{th(\ell}$$

Here, $V''_{th(i)}$ ($i = 1 - n''$) and $V''_{th(\ell)}$ denote the threshold voltages of the MOS transistors Q''_i ($i = 1 - n''$) and Q''_ℓ, respectively. Besides, the slope m' is determined by the ratio between the sum of the conductances of the MOS transistors Q_O and Q'_ℓ and the conductance of the MOS transistor Q_ℓ, and the slope m" by the ratio between the sum of the conductances of the MOS transistors Q_O, Q'_ℓ and Q''_ℓ and the conductance of the MOS transistor Q_ℓ.

Accordingly, V_O' and m' can be varied at will by n, n', $\beta(O)$, $\beta(\ell)$, $\beta'(\ell)$, $V_{th(i)}$, $V_{th(\ell)}$, $V'_{th(i)}$ and $V'_{th(\ell)}$,

while V''_O and m'' by n, n', n'', $\beta(0)$, $\beta(\ell)$, $\beta'(\ell)$, $\beta''(\ell)$, $V_{th(i)}$, $V_{th(\ell)}$, $V'_{th(i)}$, $V'_{th(\ell)}$, $V''_{th(i)}$ and $V''_{th(\ell)}$. Here, $\beta''(\ell)$ denotes the channel conductance of Q''_ℓ.

This circuit is effective when the ordinary operation range extends ~~from~~ the lower limit value V_O and the upper limit value V_O', and aging tests are carried out in the two sections of the external supply voltage $V_{CC} \geqq V_O''$ and $V_O' < V_{CC} < V_O''$. The aging tests in the two sections consist of the two operations; aging for a short time, and aging for a long time. The former serves to detect a defect occurring, for example, when an instantaneous high stress has been externally applied, while the latter serves to detect a defect ascribable to a long-time stress.

Figure 21 shows an example wherein, when the external supply voltage V_{CC} is greater than V_O', the slope m' of the voltage V_L is set at $m > m'$ under which the output voltage V_L follows up the external supply voltage V_{CC}.

Figure 22 shows an embodiment of a practicable circuit therefor. These correspond to a concrete form of the example of Figures 9 and 10. The feature of the present circuit is that a circuit DCV2 similar to DCV1 is added between the terminal 2 and ground of the circuit shown in Figure 16, whereby the conductance of a load for the transistor Q_O is increased at V_O' so as to decrease the slope of V_L.

With the present circuit, the second control starting voltage V_O' is expressed by:

$$V_O' = -\frac{1-m}{m} V_O + \left\{\sum_{i=1}^{n'} V'_{th(i)} + V'_{th(\ell)}\right\} / m$$

In addition, the slope m' is expressed by the ratio between the conductance of Q_O and the sum of the conductances of Q_ℓ and Q'_ℓ.

Accordingly, V_O' and m' can be varied at will by n, n', $\beta(O)$, $\beta(\ell)$, $\beta'(\ell)$, $V_{th(i)}$, $V_{th(\ell)}$, $V'_{th(i)}$ and $V'_{th(\ell)}$.

This circuit is applicable to devices of lower breakdown voltages. Usually, when the breakdown voltages of devices are low, the output voltage V_L of the ordinary operation region ($V_O < V_{CC} < V_O'$) may be suppressed to a low magnitude. In some cases, however, the magnitude of V_L cannot be lowered because the operating speeds of a circuit employing small geometry devices and a circuit employing large geometry devices are matched. In such cases, the slope m_a of the output voltage V_L in the ordinary operation region is made greater than m indicated in Figure 17 so as to bring V_L closer to the change of the external supply voltage. When the ordinary operation region has been exceeded, the slope of V_L is decreased in order for the aging operation point to be passed. Thus, the magnitude of the output voltage V_L

can be raised near to the withstand voltage limit of the devices within the range of the ordinary operation region, and the operating speed of the circuit employing the small geometry devices can be matched with that of the circuit employing the large geometry devices.

In an example shown in Figure 23, a characteristic in which the slope of V_L becomes m" smaller than m' when the external supply voltage V_{CC} has reached V_O" is further added to the characteristic illustrated in Figure 17.

Figure 24 shows an embodiment of a practicable circuit therefor. This corresponds to an example in which the examples of Figures 7 and 9 coexist. The feature of the present circuit is that the embodiments of Figures 18 and 21 are combined thereby to increase and decrease the slope of V_L at the two points V_O' and V_O'' respectively.

With the present circuit, the second and third control starting voltages V_O' and V_O'' are respectively expressed by:

$$V_O' = V_O + \left\{\sum_{i=1}^{n'} V'_{th(i)} + V'_{th(\ell)}\right\}/(1 - m)$$

$$V_O'' = V_O' + \left\{\sum_{i=1}^{n''} V''_{th(i)} + V''_{th(\ell)} + \sum_{i=1}^{n'} V'_{th(i)} + V'_{th(\ell)} - V_O'\right\}/m'$$

In addition, the slope m' is expressed by the ratio between the sum of the conductances of Q_O and $Q_\ell{}'$ and the conductance of Q_ℓ, while m'' is expressed by the ratio between the sum of the conductances of Q_O and $Q_\ell{}'$ and the sum of the conductances of Q_ℓ and $Q_\ell{}''$.

Accordingly, $V_O{}'$ and m' can be varied at will by n, n', $\beta(O)$, $\beta(\ell)$, $\beta'(\ell)$, $V_{th(i)}$, $V_{th(\ell)}$, $V'_{th(i)}$ and $V'_{th(\ell)}$, while $V_O{}''$ and m'' can be varied by n, n', n'', $\beta(O)$, $\beta(\ell)$, $\beta'(\ell)$, $\beta''(\ell)$, $V_{th(i)}$, $V_{th(\ell)}$, $V'_{th(i)}$, $V'_{th(\ell)}$, $V''_{th(i)}$ and $V''_{th(\ell)}$.

This circuit protects small geometry devices from permanent breakdown in such a way that, even when V_{CC} has become higher than the withstand voltage limit $V_O{}''$ of the devices due to ~~any~~ some fault of the external power source, it does not exceed a breakdown voltage V_B. That is, the slope m'' of V_L for V_{CC} not smaller than $V_O{}''$ is made gentler than the slope m' in the aging, whereby even when the external supply voltage V_{CC} has become $V_O{}''$ or above, the output voltage V_L is prevented from exceeding the breakdown voltage (usually, higher than the withstand voltage limit) of the devices. This makes it possible to prevent the device breakdown even when the supply voltage has been raised abnormally by way of example.

Figure 25 shows an example in which the slope m' is made negative when the external supply voltage V_{CC} has exceeded $V_O{}'$.

Figure 26 shows an embodiment of a practical circuit therefor. These correspond to a concrete form of the example of Figures 11 and 12. The feature of the present circuit is that the drain of Q_1' in DCV2 is connected to the terminal 1 of the circuit shown in Figure 16, the drain of Q_ℓ' to the terminal 2, and the source of Q_ℓ' to the ground, whereby the conductance of Q_ℓ' is controlled by V_{CC}, and besides, it is made greater than the conductance of Q_0 so as to establish $m' < 0$.

With the present circuit, the second control starting voltage V_0' and the slope m' are expressed by the following on the assumption of $\beta'(\ell) \gg \beta(0)$:

$$V_0' = \sum_{i=1}^{n'} V'_{th(i)} + V'_{th(\ell)}$$

$$m' = 1 - \sqrt{\beta'(\ell)/\beta(0)}$$

Accordingly, V_0' and m' can be varied at will by n', $V'_{th(i)}$, $V'_{th(\ell)}$ and $\beta'(\ell)/$ (0).

Figures 27 and 28 show a practicable example of the present circuit and examples of the characteristics thereof. All the threshold voltages of transistors are 1 (one) V, and $V_G = V_{CC} + V_{th(0)}$ is held. In addition, numerals in parentheses indicate values obtained by dividing the channel widths by the channel lenghts of the transistors. Figure 28 illustrates V_L with a parameter being the corresponding value W_ℓ/L_ℓ of Q_ℓ'. By way of

example, the voltage in the ordinary operation is set at 5 V, and the aging voltage at 8 V.

This circuit consists in that the slope of the voltage at and above V_O'' in the characteristic shown in Figure 23 is made negative, thereby to intensify the aspect of the device protection of the circuit in Figure 24.

With this circuit, the breakdown due to the external application of a high voltage is perfectly prevented, and the power consumption in the integrated circuit does not exceed an allowable value. Thus, even when the instantaneous high voltage has been externally applied, the prevention of the breakdown of the devices is ensured.

Thus far, the voltage converters and their characteristics have been described. Next, the method of feeding the voltage converter with power will be described.

b In the above, the gate voltage of Q_O has been presumed to be ~~supposed~~ $V_{CC} + V_{th}$. This has intended to simplify the computation and to clearly elucidate the characteristics of the circuits. Essentially, however, this voltage need not

b be limited ~~stuck~~ to $V_{CC} + V_{th}$, but may be chosen at will for the convenience of design.

Figure 29(A) shows a practicable circuit which boosts the gate voltage V_G to above the supply voltage V_{CC} within the chip as stated with reference to Figure 15.

When a pulse ϕ_i of amplitude V_{CC} from an oscillator OSC included within the chip rises from 0 (zero) V to V_{CC}, a node 4' having been previously charged to $V_{CC} - V_{th}$ by Q_1' is boosted to $2\ V_{CC} - V_{th}$.

In consequence, a node 4 becomes a voltage $2\ (V_{CC} - V_{th})$ lowered by V_{th} by means of Q_2'. Subsequently, when ϕ_i becomes 0 V and a node 2 rises to V_{CC}, the node 4 is further boosted into $3\ V_{CC} - 2\ V_{th}$. Accordingly, a node 5 becomes a voltage $3\ (V_{CC} - V_{th})$ lowered by V_{th} by means of Q_2. Each of Q_2' and Q_2 is a kind of diode, so that when such cycles are continued a large number of times, V_G becomes a D.C. voltage of $3\ (V_{CC} - V_{th})$. V_G of higher voltage is produced by connecting the circuits CP1, CP2 in a larger number of stages. The reason why the two stages are comprised here, is as follows. Assuming V_{CC} to lower to 2.5 V and V_{th} to be 1 (one) V, one stage affords $V_G = 2\ (V_{CC} - V_{th})$, and hence, $V_G = 3$ V holds. Under this condition, however, the source voltage V_L of Q_O in Figure 15 becomes 2 V lower than V_{CC}. In contrast, when the two stages are disposed, $V_G = 4.5$ V holds because of $V_G = 3\ (V_{CC} - V_{th})$. Accordingly, V_L can be equalized to V_{CC}, so that $V_L = V_{CC}$ can be established below V_O as in Figure 15. Conversely, however, as V_{CC} becomes a higher voltage, V_G may ~~is more feared to~~ become an excess voltage which can ~~and to~~ break down the associated transistors.

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b Therefore, ~~any~~ some circuit for limiting V_G is required on the high voltage side of V_{CC}.

Figure 30 shows an example in which $V_G \simeq 3\ (V_{CC} - V_{th})$ is held as a high voltage on the low voltage side of V_{CC}, and besides, $V_{CC} + 2\ V_{th}$ is held on the high voltage side of V_{CC} in order to protect the associated transistors. Here, any of the circuits thus far described, for example, the whole circuit in Figure 16, 18, 20, 22, 24 or 26, is indicated by LM1 as the load of V_G. A protection circuit CL1 is such that, when V_G is going to exceed $V_{CC} + 2\ V_{th}$, current flows through Q_1 and Q_2, so V_G results in being fixed to $V_{CC} + 2\ V_{th}$. With the present circuit, V_{CC} at which CL1 operates ranges from $3\ (V_{CC} - V_{th}) = V_{CC} + 2\ V_{th}$ to $V_{CC} = 5/2 V_{th}$.

Figure 31 shows a practicable circuit of the inverter 1 or 2 in Figure 29(A). An output pulse ϕ_0 is impressed on the circuit CP1 or CP2.

While the oscillator OSC can be constructed as a circuit built in the chip, Figure 32 shows an example utilizing a back bias generator which is built in the chip in order to apply a back bias voltage V_{BB} to a silicon substrate. The advantage of this example is that the oscillator need not be designed anew, which is effective for reducing the area of the chip. In general, when V_L is applied to respective transistors

with V_{BB} being O (zero) V, the threshold voltages V_{th} of the respective transistors are not normal values. Therefore, an excess current flows, or stress conditions on the transistors become severe, so the transistors can break down. In contrast, when this circuit is used, V_{BB} is generated upon closure of a power source, and V_L is generated substantially simultaneously, so that the operations of respective transistors are normally executed.

Next, practicable embodiments of buffer circuits will be described. As the load of the voltage converter, there is sometimes disposed a load of large capacity or of great load fluctuation. In this case, such heavy load needs to be driven through a buffer circuit of high driving ability. As a realizing expedient therefor, the ordinary method is considered in which the load is driven through a single transistor of high driving ability, namely, great W/L as shown in Figure 33. With this method, however, the performance degrades because a voltage drop of V_{th} arises on the low voltage side of V_{CC} as shown in Figure 34. Figure 35 shows a practicable example of the buffer circuit which has a high driving ability without the V_{th} drop. When a voltage V_{PP} is made greater than $V_L + V_{th}$ and a resistance R_P is made much higher than the equivalent "on" resistance of a

transistor Q_1, the gate voltage of a transistor Q_2 becomes $V_L + V_{th}$. Accordingly, the source voltage V_{L1} of Q_2 equalizes to V_L. When the W/L of Q_2 is made great, the desired buffer circuit is provided. Here, V_L becomes V_{CC} on the low voltage side of V_{CC}, so that V_{PP} must be at least $V_{CC} + V_{th}$. As a circuit therefor, the circuit shown in Figure 29(A) is usable. Regarding connection, the node 5 of the circuit in Figure 29(A) may be connected to the drain of Q_1 in a regulator in Figure 35. Here, in order that the effective output impedance as viewed from the node 5 may be made sufficiently higher than the equivalent "on" resistance of Q_1 of the circuit in Figure 35, the value of the W/L of Q_2 or the value of C_B in Figure 29(A) or the oscillation frequency of OSC may be properly adjusted by way of example.

As to some loads, it is necessary to apply V_L to the drain of a transistor constituting a part of the load and to apply $V_L + V_{th}$ to the gate thereof, so as to prevent the V_{th} drop and to achieve a high speed operation. Figure 36 shows an embodiment therefor. The circuit LM_1 is, for example, the circuit in Figure 16, and the voltage V_{L1} equalizes to V_L as stated before. In addition, the gate voltage of Q_4 is $V_L + 2\ V_{th}$. Therefore, V_{L2} becomes $V_L + V_{th}$. Here, transistors Q_6 and Q_7 serve to prevent unnecessary charges from remaining in V_{L1}

at the transient fluctuation of V_{CC}. Q_6 and Q_7 are connected into LM1 as shown in the figure so as to operate at V_{CC} of at least V_O and at V_{CC} of at least $V_O - V_{th}$. Here, the ratio W/L of Q_6, Q_7 is selected to be sufficiently smaller than that of Q_2, to minimize the influence of the addition of Q_6, Q_7 on V_L. It has been previously stated that Q_7 operates in the region not greater than V_O. Since Q_2 and Q_4 are in the operating states of unsaturated regions ($V_{GS} - V_{th} \geq V_{DS}$, V_{GS}: gate-source voltage, V_{DS}: drain-source voltage) in the region not greater than V_O, surplus charges are discharged to V_{CC} through Q_2, Q_4, and hence, Q_7 is unnecessary in principle. However, when V_{CC} is near V_O, the "on" resistances of Q_2, Q_4 increase unnecessarily, and it is sometimes impossible to expect the effects of these transistors. Accordingly, Q_7 is added, whereby stable values of V_{L1} can be obtained in a wide range from the region ($V_O - V_{th}$) where V_{CC} is not greater than V_O, to the region where V_{CC} is greater than V_O and where the converter is normally operating.

The function of Q_5 is that, when V_{L1} is going to fluctuate negatively relative to V_{L2}, current flows to Q_5 so as to keep the difference of V_{L2} and V_{L1} constant. In addition, in the present embodiment, the example of V_L and $V_L + V_{th}$ has been stated. However, when the pairs of Q_1, Q_2 or the pairs of Q_3, Q_4 are connected

in cascade, a voltage whose difference from V_{L1} becomes an integral multiple ~~times~~ of V_{th} can be generated.

A circuit shown in Figure 37 is another buffer circuit which is connected to the output stage of the circuit of Figure 35 or 36 in order to further ~~more~~ enhance the driving ability of the buffer circuit of Figure 35 or 36. By connecting such a buffer circuit of higher driving ability, a large load capacity can be driven. B7 First, V_{L1} becomes $V_{L1} + 2\ V_{th}$ and $V_{L1} + V_{th}$ at respective nodes 4 and 2. Eventually, however, it is brought into V_{DP} being the level of V_{L1} at a node 5 by Q_4. B8 ~~Problematic here is the load driving ability of Q_4 which serves to charge a large capacitance C_D in the load LC1 at high speed.~~ In order to enhance the ability, the node 2 being the gate of Q_4 needs to be boosted in a time zone for charging the load. B9 Transistors ~~therefor are~~ Q_6 - Q_{11}, and capacitors are C_1 and C_2. B10 A node 6 discharged by Q_{13} owing to the "on" state of ϕ_2 is charged by Q_{12} and Q_4 when the next ϕ_1 is in the "on" state ~~is "on"~~. At this time, the node 2 being at $V_{L1} + V_{th}$ and a node 3 being at V_{L1} are boosted by the "on" state of ϕ_1. Consequently, the conductances of Q_{10}, Q_{11} increase, so that the boosted voltage of the node 2 is discharged to the level of $V_{L1} + V_{th}$ by Q_{10}, Q_{11}. Here, when the boosting time is made longer than the charging time of C_D based on Q_4, Q_{12}, the capacitor C_D is charged

~~fast~~ rapidly. The transistor Q_6 cuts off the nodes 3 and 1 when the node 3 is boosted by control signal ϕ_1. When control signal ϕ_2 is "on", Q_7 - Q_9 turn "off" subject to the condition of $V_{L1} \leqq 3\ V_{th}$, so that Q_{11} has its gate rendered below V_{th} to turn "off". Accordingly, no current flows through Q_3, Q_{10} and Q_{11}, so that the power consumption can be rendered low. In addition, in order to reduce the power consumption in the case of $V_{L1} > 3\ V_{th}$, the "on" resistance of Q_6 may be increased to lower current. The voltage of the node 3 at this time becomes a stable value of approximately $3\ V_{th}$. Thus, the boosting characteristic of the node 3 is also stabilized, with the result that the operation of the whole circuit can be stabilized.

Here, since the sources and gates of Q_7 and Q_{10} are connected in common, the conditions of biasing the gates are quite equal. Accordingly, when

$$\frac{\text{capacitance of node } \overset{3}{\cancel{2}}}{(W/L)\ Q_7} = \frac{\text{capacitance of node } \overset{2}{\cancel{3}}}{(W/L)\ Q_{10}}$$

is held in advance, the boosting characteristics of the nodes 2, 3 can be made quite equal, so the circuit design can be facilitated advantageously. That is, one merit of the present embodiment consists in that the boosting characteristic of the node 2 can be automatically controlled with the boosting characteristic of the node 3. In this way, the D.C. path from the node 2 to V_{SS}

in the case of performing no boosting can be relieved, and it becomes possible to lower the power consumption.

Here, Q_5 has the function of discharging the surplus charges of the node 2 when Q_{10} is "off".

As regards the embodiment of Figure 37, various modifications can be considered. While the drain of Q_6 in Figure 37 is connected to V_{L1} in order to stabilize the boosting characteristics of the nodes 2, 3 to the utmost, it can also be connected to V_{CC} so as to relieve a burden on V_{L1}. Likewise, while Q_{10} subject to the same operating condition as that of Q_7 is disposed in order to stabilize the boosting characteristics of the nodes 2, 3, it may well be removed into an arrangement in which the nodes 2 and 9 are directly connected, with the source of Q_7 and the node 9 disconnected. Since, in this case, the relationship of Q_9 and Q_{11} is in the aforementioned relationship of Q_7 and Q_{10}, the boosting characteristics can be similarly designed, and the occupying area of the circuit can be effectively reduced. Further, the 3-stage connection arrangement of Q_7, Q_8 and Q_9 is employed here. This is a consideration for efficiently forming the circuit in a small area by utilizing a capacitance C_2 (for example, the capacitance between the gate of a MOST and an inversion layer formed between the source and drain thereof, known from ISSCC 72 Dig. of Tech. Papers, p. 14, etc.) for the

reduction of the power consumption described above. That is, in order to use the inversion layer capacitance, the gate voltage to be applied needs to be higher by at least V_{th} than the source and drain. Accordingly, in case of forming C_2 by the use of a MOST of low V_{th} or an ordinary capacitor, it is also possible to reduce the connection number of $Q_7 - Q_9$ to two or one.

The buffer circuit as shown in Figure 37 is indispensable especially to the LSI systems as shown in Figures 1 and 2. In general, the voltage converter for generating V_L in Figure 1 or 2 is desired to have an especially high ability of supplying current because the circuit current in the circuit A, A' or B flows toward the ground. Accordingly, when the whole circuit including the circuit of Figure 37 thus far described is regarded as the voltage converter of Figure 1 or 2, it is applicable to general LSIs.

With the embodiments stated above, when the actual circuit of Figure 18 which is diode-connected as shown in Figure 27 is operated at V_{CC} of or above V_O as shown in Figure 17, current flows through $Q_1' - Q_S'$ (Figure 27) to increase the power consumption. This increase of the power consumption poses a problem in case of intending to back up the LSI power source, namely, the externally applied supply voltage with a battery. More specifically,

in an apparatus wherein the ordinary external power source is backed up by a battery when turned "off"; when the power consumption of the LSI itself is high, the period of time for which the power source is backed up is limited because the current capacity of the battery is small. Therefore, with a measure wherein V_{CC} to be applied by the battery is set at below V_O during the time interval during which the battery is operated for backup, no current flows through $Q_1' - Q_S'$, and hence, the period of time for which the power source can be backed up can be extended to that extent. Alternatively, the number of stages of $Q_1' - Q_S'$ (Figure 27) can be determined so as to establish V_O which is greater than V_{CC} being the battery supply voltage in the case of the backup.

The supply voltage V_{CC} in the ordinary operation can be selected at $V_{CC} < V_O$ besides at $V_{CC} > V_O$. Since this permits no current to flow through $Q_1' - Q_S'$ under the ordinary V_{CC} condition, the power consumption can be lowered. Another merit is that design is facilitated because the circuit can be designed ~~whilst~~ while avoiding a region where the relation of V_{CC} and V_L becomes a polygonal line. More specifically, when the polygonal region is used, ~~the~~ an imbalance of characteristics concerning V_{CC} arises between a circuit directly employing V_{CC} and

a part of a certain circuit employing V_L by way of example, so that the operation sometimes becomes unstable. When $V_{CC} < V_O$ holds ~~is held~~, this drawback can be eliminated.

In the above, the practicable embodiments have been described in which the voltage converters are constructed of MOS transistors. These are examples which chiefly employ MOS transistors of positive threshold voltages V_{th}, namely, of the enhancement mode. Needless to say, however, it is also possible to employ a MOS transistor of negative V_{th}, namely, of the depletion mode as disclosed in Figure 16 of Japanese Patent Application No. 56-168698. For example, in the embodiment of Figure 16, in order to establish $V_L = V_{CC}$ in the region of $V_{CC} \leq V_O$ as illustrated in the characteristic of Figure 15, the gate voltage of Q_O needs to be $V_G \geq V_{CC} + V_{th(O)}$, and it has been stated that the circuit of Figure 29(A) may be used as the V_G generator therefor. In this regard, the circuit can be further ~~more~~ simplified by employing the MOS transistor of the depletion mode. Figure 39 shows such a practicable embodiment. It differs from the circuit of Figure 16 in that Q_O is replaced with the depletion mode MOS transistor Q_O', the gate of which is connected to the terminal 2. With this measure, since the $V'_{th(O)}$ of Q_O' is negative, Q_O' is in the "on" state at all times, and the desired characteristic illustrated in Figure 15 can be realized

without employing the V_G generator as shown in Figure 29(A). With the present embodiment, not only the circuit arrangement can be simplified as stated above, but also the merit of attaining a stable characteristic is achieved because current $I(Q_O')$ to flow through Q_O' becomes a constant current determined by $\beta'(O)$ (channel conductance) and $V'_{th(O)}$ (threshold voltage) as $I(Q_O') = \frac{\beta'(O)}{2} \cdot V'_{th(O)}{}^2$. Although the present embodiment has exemplified Figure 16, it is applicable as it is by substituting Q_O' for Q_O in any other embodiment and connecting its gate to the terminal 2 as in the present embodiment.

Figure 40 shows an embodiment in which a buffer circuit is constructed using a single depletion-mode MOS transistor, while Figure 41 shows the characteristic thereof. Although the present embodiment is the same in the circuit arrangement as the foregoing embodiment of Figure 33, it differs in that the MOS transistor is changed from the enhancement mode into the depletion mode. As shown in Figure 41, the output V_L' of the present buffer circuit bends from a point P at which the difference of V_{CC} and V_L equalizes to the absolute value $|V_{thD}|$ of the threshold voltage V_{thD} of the MOS transistor, and it thereafter becomes a voltage which is higher than V_L by $|V_{thD}|$. Accordingly, V_L may be set lower than a desired value by $|V_{thD}|$. The present

embodiment has the simple circuit arrangement, and can meritoriously eliminate the problem, as in the characteristic of the embodiment of Figure 33 illustrated in Figure 34, that only the output lower than V_{CC} by V_{th} can be produced in the range of $V_{CC} \leq V_O$.

As set forth above, the present invention can provide, in an integrated circuit having small geometry devices, an integrated circuit which has a wide operating margin even against the fluctuations of an external supply voltage in an ordinary operation and which can apply a sufficient aging voltage.